

# 1 Watt Audio Power Amplifier

#### **DESCRIPTION**

The EUA4890 is an audio power amplifier designed for portable communication device applications such as mobile phone applications. The EUA4890 is capable of delivering 1.0W of continuous average power to an  $8\Omega$  BTL load with less than 1% distortion (THD+N) from a 5.0V power supply, and 350mW to a  $8\Omega$  BTL load from a 3V power supply.

The EUA4890 provides high quality audio while requiring few external components and minimal power consumption. It features a low-power shutdown mode, which is achieved by driving the SHUTDOWN pin with logic low.

The EUA4890 contains circuitry to prevent from "pop and click" noise that would otherwise occur during turn-on and turn-off transitions.

For maximum flexibility, the EUA4890 provides an externally controlled gain (with resistors), as well as an externally controlled turn-on and turn-off times (with the bypass capacitor).

The EUA4890 is available in a MSOP-8 and a 3mm×3mm QFN package.

#### **FEATURES**

- 2.5-5.5V operation
- 65dB PSRR at 217Hz, V<sub>DD</sub>=5V
- 0.1µA ultra low current shutdown mode
- Improved pop & click circuitry
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Thermal shutdown protection
- Unity-gain stable
- External gain configuration capability
- BTL output can drive capacitive loads

#### **APPLICATIONS**

- Mobile Phones
- PDAs
- Portable electronic devices

#### **Block Diagram**

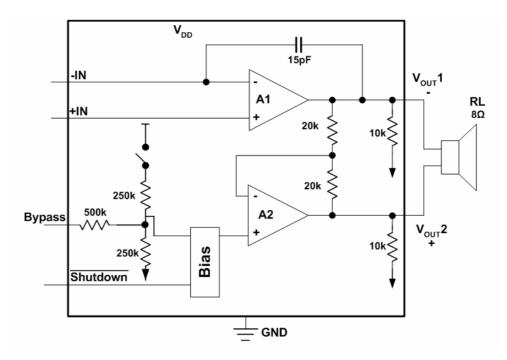


Figure 1.



### **Typical Application Circuit**

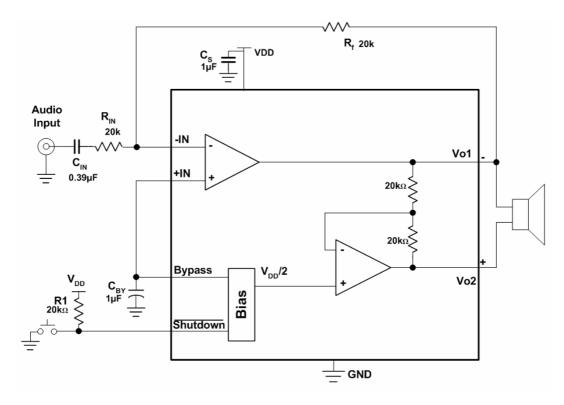


Figure 2. Audio Amplifier with Single-Ended Input

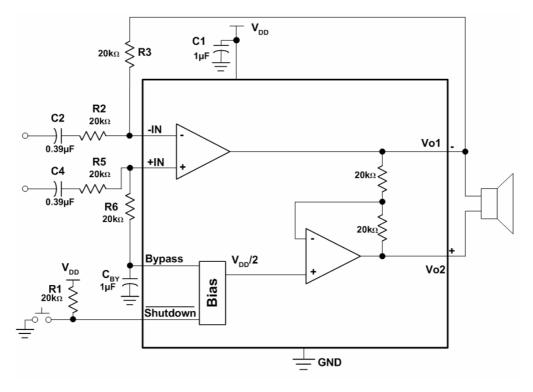
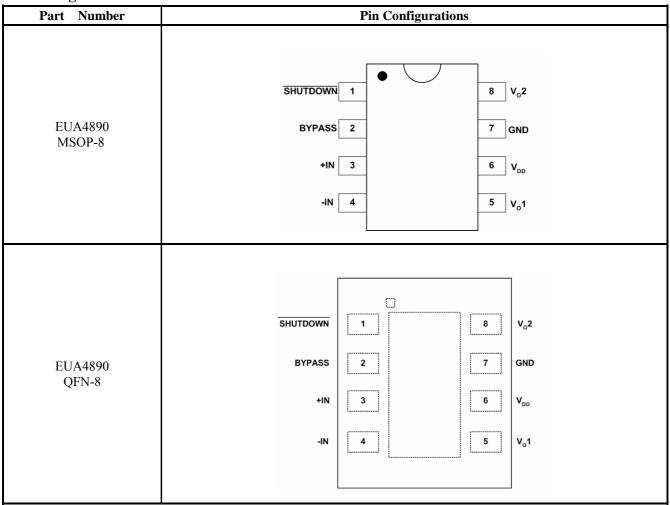


Figure 3. Audio Amplifier with Differential Input



#### **Pin Configurations**



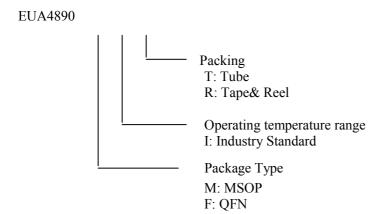
### **Pin Description**

PIN	PIN	I/O	DESCRIPTION
SHUTDOWN	1	I	The device enters in shutdown mode when a low level is applied on this pin
BYPASS	2	I	Bypass capacitor pin which provides the common mode voltage
+IN	3	I	Positive input of the first amplifier, receives the common mode voltage
-IN	4	I	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor $R_f$ and to the input resistor $R_{in}$ .
V <sub>O1</sub>	5	О	Negative output of the EUA4890. Connected to the load and to the feedback resistor $R_{\rm f}$
$V_{\scriptscriptstyle DD}$	6	I	Analog V <sub>DD</sub> input supply.
GND	7		Ground connection for circuitry.
$V_{O2}$	8	О	Positive output of the EUA4890.

EUTECH

## **Ordering Information**

Order Number	Package Type	Marking	Operating Temperature range
EUA4890MIT	MSOP-8	xxxx A4890	-40 °C to 85°C
EUA4890MIR	MSOP-8	xxxx A4890	-40 °C to 85°C
EUA4890FIT	QFN-8	xxxx A4890	-40 °C to 85°C
EUA4890FIR	QFN-8	xxxx A4890	-40 °C to 85°C





## **Absolute Maximum Ratings**

Supply voltage, V <sub>DD</sub>	6V
Input voltage, $V_{I}$	-0.3 V to $V_{DD}$ +0.3 V
Storage temperature rang, T <sub>stg</sub>	65°C to 150°C
ESD Susceptibility	2kV
Junction Temperature	150°C
Thermal Resistance	
$\theta_{JC}$ (MSOP)	56°C/W
$\theta_{JA}$ (MSOP)	160°C/W
θ <sub>JA</sub> (QFN)	50°C/W

# Electrical Characteristics $V_{DD}=5V,\,T_A=25^{\circ}C$

Symbol	Parameter	Conditions	EUA4890			Unit
Symbol	i ai ametei	Conditions	Min	Typ	Max.	Omt
T	Quiescent Power Supply Current	$V_{IN}=0V$ , $I_O=0A$ , No load		2.4	5	mA
$I_{DD}$	Quiescent i ower suppry current	$V_{IN}$ =0V, $I_{O}$ =0A, $8\Omega$ load		2.5	5	mA
$I_{SD}$	Shutdown Current	V <sub>SHUTDOWN</sub> =0V		0.1	2.0	μΑ
$V_{\mathrm{SDIH}}$	Shutdown Voltage Input High		1.2			V
$V_{ m SDIL}$	Shutdown Voltage Input Low				0.4	V
Vos	Output Offset Voltage			5	25	mV
R <sub>OUT-GND</sub>	Resistor Output to GND		7.0	8.5	9.7	kΩ
$P_{\rm O}$	Output Power $(8\Omega)$	THD=1%; f=1kHz		1.1		W
$T_{ m WU}$	Wake-up time			170	220	ms
$T_{SD}$	Thermal Shutdown Temperature		150	170		°C
THD+N	Total Harmonic Distortion + Noise	P <sub>O</sub> =0.4 Wrms; f=1kHz		0.15		%
PSRR	Power Supply Rejection Ratio	Vripple=200mV sine p-p Input Terminated with 10 ohms to ground	55	65(f=217 Hz) 67(f=1kH z)		dB
$T_{SDT}$	Shutdown Time	8Ω load		1.0		ms



# Electrical Characteristics VDD = 3V, $T_A = 25^{\circ}C$

Symbol	Parameter	Conditions	]	Unit			
Symbol	Farameter	Conditions	Min	Typ	Max.	Omt	
$I_{ m DD}$	Quiescent Power Supply Current	$V_{IN}$ =0V, $I_{O}$ =0A, No load		1.8	4	mA	
1DD	Quiescent I ower Suppry Current	$V_{IN}$ =0V, $I_{O}$ =0A, $8\Omega$ load		1.9	4	mA	
$I_{SD}$	Shutdown Current	V <sub>SHUTDOWN</sub> =0V		0.1	2.0	μΑ	
$V_{\mathrm{SDIH}}$	Shutdown Voltage Input High		1.2			V	
$V_{\mathrm{SDIL}}$	Shutdown Voltage Input Low				0.4	V	
$V_{OS}$	Output Offset Voltage			5	25	mV	
R <sub>OUT-GND</sub>	Resistor Output to GND		7.0	8.5	9.7	kΩ	
Po	Output Power $(8\Omega)$	THD=1%; f=1kHz	0.28	0.35		W	
$T_{WU}$	Wake-up time			120	180	ms	
$T_{SD}$	Thermal Shutdown Temperature		150	170		°C	
THD+N	Total Harmonic Distortion + Noise	P <sub>O</sub> =0.15 Wrms; f=1kHz		0.15		%	
PSRR	Power Supply Rejection Ratio	Vripple=200mV sine p-p Input Terminated with 10 ohms to ground	45	65(f=217 Hz) 66(f=1kH z)		dB	

## Electrical Characteristics $V_{DD}$ = 2.6V, $T_{A}$ = 25 $^{\circ}C$

Symbol	Parameter	Conditions	EUA4890			Unit
Symbol	rarameter	Conditions	Min	Typ	Max.	Omt
$I_{DD}$	Quiescent Power Supply Current	$V_{IN}$ =0V, $I_{O}$ =0A, No load		1.7		mA
$I_{SD}$	Shutdown Current	V <sub>SHUTDOWN</sub> =0V		0.1		μΑ
Po	Output Power (8 $\Omega$ ) Output Power (4 $\Omega$ )	THD=1%; f=1kHz THD=1%; f=1kHz		0.25 0.32		W
THD+N	Total Harmonic Distortion + Noise	P <sub>O</sub> =0.1Wrms; f=1kHz		0.15		%
PSRR	Power Supply Rejection Ratio	Vripple=200mV sine p-p Input Terminated with 10 ohms to ground		55(f=217 Hz) 56(f=1kH z)		dB



#### **Typical Operating Characteristics**

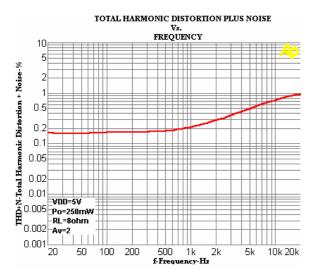


Figure 3.

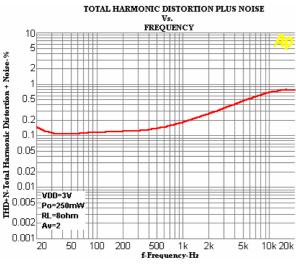
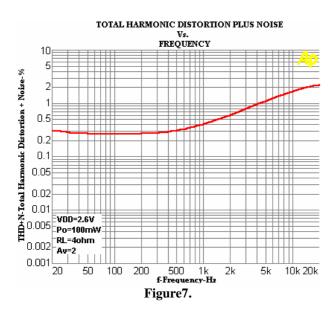
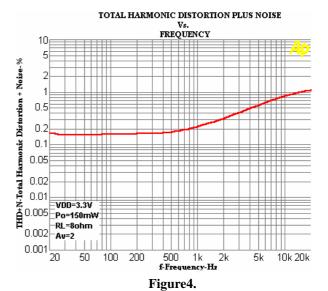
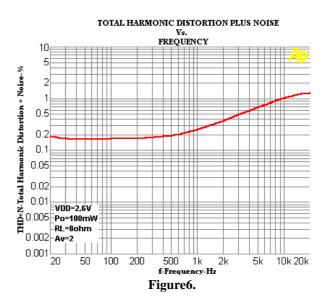
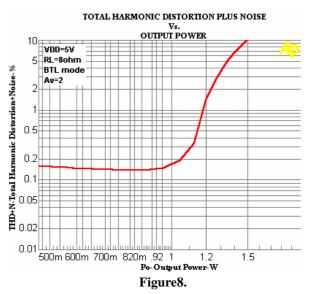


Figure 5.

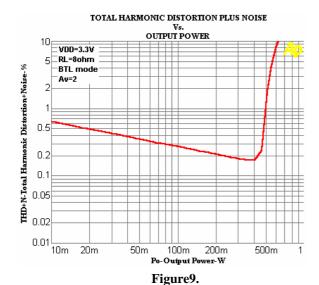


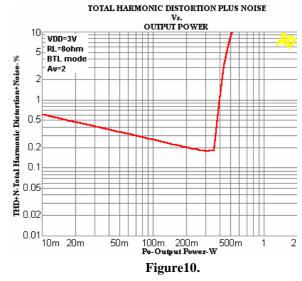


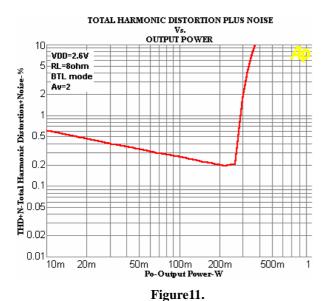


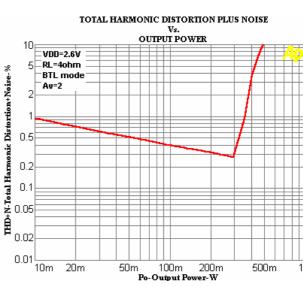


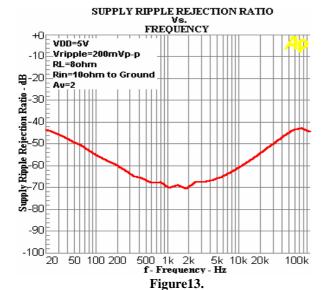
EUTECH



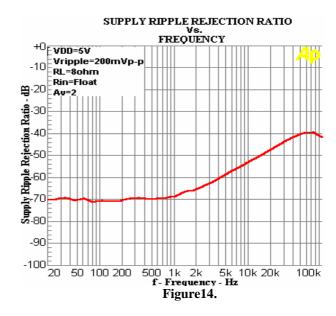




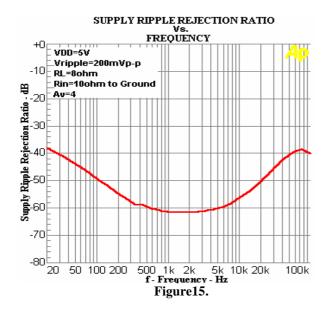


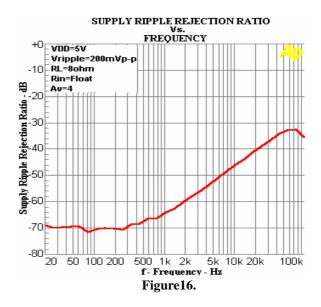


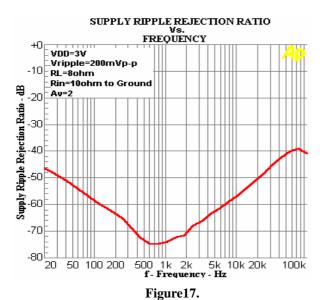


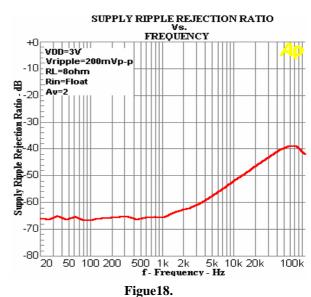


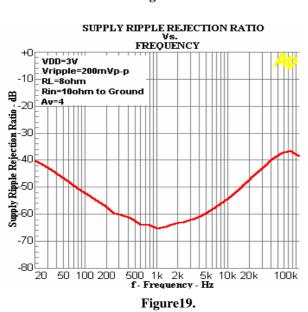


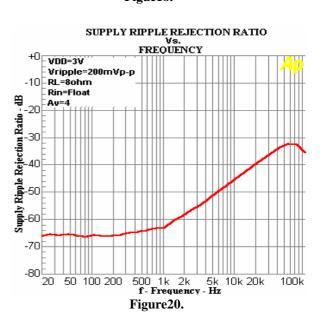


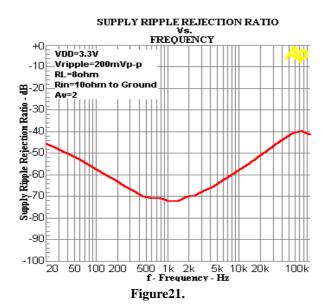












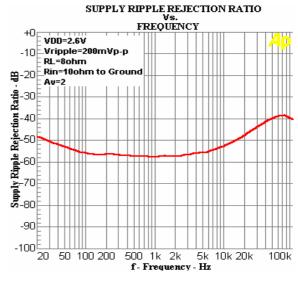


Figure 22.

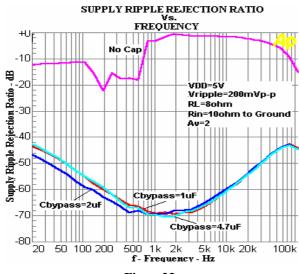
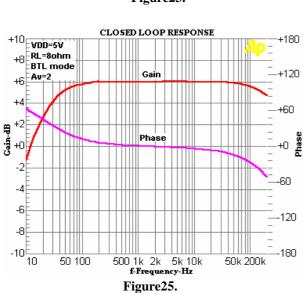


Figure 23.



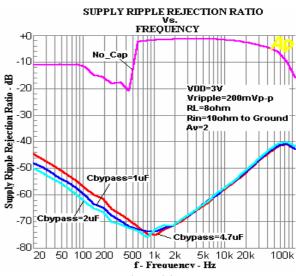
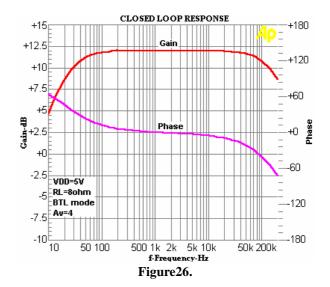
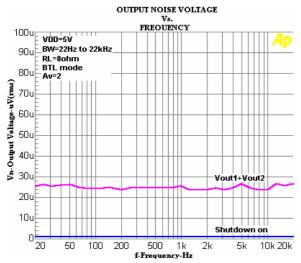


Figure 24.





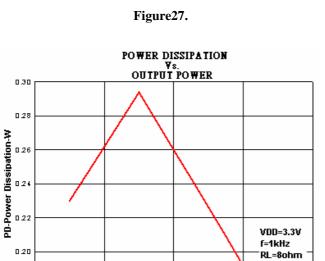


Figure 29.

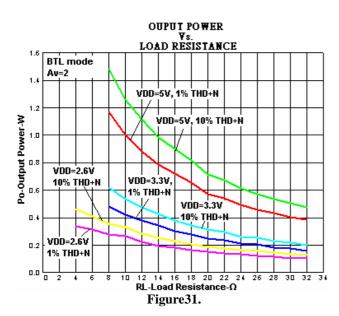
Po-Output Power-W

0.2

BTL mode

0.8

0.6



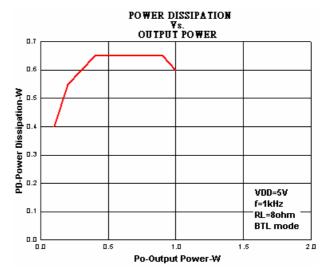


Figure 28.

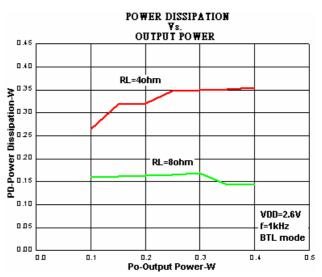


Figure 30.

EUTECH

11

0.18

#### **Application Information**

#### **Bridged Configuration Explanation**

The structure of the EUA4890 is basically composed of two identical internal power amplifiers; the first one is externally configurable with gain-setting resistors Rin and Rf (the closed-loop gain is fixed by the ratios of these resistors) and the second is internally fixed in an inverting unity-gain configuration by two resistors of  $20k\Omega$ . So the load is driven differentially through OUTA and OUTB outputs. This configuration eliminates the need for an output coupling capacitor.

The differential-ended amplifier presents two major advantages:

- The possible output power is four times larger (the output swing is doubled) as compared to single-ended amplifier under the same conditions.
- Output pins (OUTA and OUTB) are biased at the same potential V<sub>DD</sub>/2, this eliminates the need for an output coupling capacitor required with a single-ended amplifier configuration.

The differential closed loop-gain of the amplifier is

given by Avd= 
$$2 \times \frac{R_f}{Rin} = \frac{Vorms}{Vinrms}$$

#### **Power Dissipation**

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the EUA4890 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs of from equation1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L)$$
 -----(1)

It is critical that the maximum junction temperature  $T_{\rm JMAX}$  of 150°C is not exceeded.  $T_{\rm JMAX}$  can be determine from the power derating curves by using  $P_{\rm DMAX}$  and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher  $P_{\rm DMAX}$ . Additional copper foil can be added to any of the leads connected to the EUA4890.If  $T_{\rm JMAX}$  still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power.

#### **Proper Selection of External Components**

The EUA4890 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor and proper bypassing capacitor in the typical application.

#### Gain-Setting Resistor Selection (Rin and Rf)

 $R_{\rm in}$  and  $R_{\rm f}$  set the closed-loop gain of the amplifier. In order to optimize device and system performance, the EUA4890 should be used in low gain configurations.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs.

A closed loop gain in the range from 2 to 5 is recommended to optimize overall system performance. An input resistor  $(R_{\rm in})$  value of  $20k\Omega$  is realistic in most of applications, and does not require the use of a too large capacitor  $C_{\rm in}.$ 

#### Input Capacitor Selection (Cin)

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high-pass filter with R<sub>in</sub>, the cut-off frequency is given by

$$fc = \frac{1}{2 * \Pi * R_{in} * C_{in}}$$

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation. However a large input coupling capacitor requires more time to reach its quiescent DC voltage  $(V_{\rm DD}/2)$  and can increase the turn-on pops.

An input capacitor value between  $0.1\mu$  and  $0.39\mu F$  performs well I many applications (with  $R_{in}$ =20k $\Omega$ ).

#### **Bypass Capacitor Selection (Cby)**

The bypass capacitor C<sub>by</sub> provides half-supply filtering and determines how fast the EUA4890 turns on.

This capacitor is critical component to minimize the turn-on pop. A  $1.0\mu F$  bypass capacitor value ( $C_{in}$  = <  $0.39\mu F$ ) should produce clickless and popless shutdown transitions. The amplifier is still functional with a  $0.1\mu F$  capacitor value but is more susceptible to pop and click noise. Thus, a  $1.0\mu F$  bypassing capacitor is recommended.

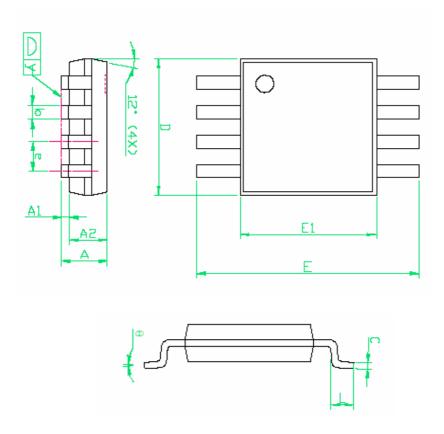
#### Power Supply Bypassing (C<sub>S</sub>)

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device s possible.



### **Packaging Information**

#### MSOP-8



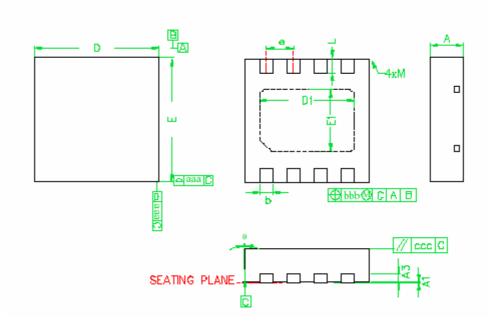
#### NOTE

- 1. Package body sizes exclude mold flash and gate burrs
- 2. Dimension L is measured in gage plane
- 3. Tolerance 0.10mm unless otherwise specified
- 4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
STWIDOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.0375	0.043
A1	0.05	0.09	0.15	0.002	0.004	0.006
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.28	0.30	0.38	0.011	0.012	0.015
С	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
Е	4.70	4.90	5.10	0.185	0.193	0.201
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.026	
L	0.40	0.53	0.66	0.016	0.021	0.026
y			0.10			0.004
	0		6	0		6

EUTECH

#### QFN-8



#### NOTE

- 1. All dimensions are in millimeters,  $\theta$  is in degrees
- 2. M: The maximum allowable corner on the molded plastic body corner
- 3. Dimension D does not include mold protrusions or gate burrs. Mold protrusions and gate burrs shall not exceed 0.15mm per side
- 4. Dimension E does not include interterminal mold protrusions or terminal protrusions. Interminal mold protrusions and/or terminal protrusions shall not exceed 0.20mm per side
- 5. Dimension b applies to plated terminals. Dimension A1 is primarily Y terminal plating, but may or may not include a small protrusion of terminal below the bottom surface of the package
- 6. Burr shall not exceed 0.060mm
- 7. JEDEC MO-229

SYMBOLS	DIMENSIONS IN MILLIMETERS				
	MIN.	NOM.	MAX.		
A	0.81	0.9	1.00		
A1	0	0.015	0.03		
A3		0.20 REF			
В	0.25	0.30	0.37		
D	2.85	3.00 BSC	3.15		
D1		2.3 BSC			
Е	2.85	3.00 BSC	3.15		
E1		1.5 BSC			
e		0.65 BSC			
L	0.25	0.35	0.45		
aaa		0.25			
bbb		0.10			
ccc		0.10			
M			0.05		
θ	-12		0		

EUTECH