eMPIA Technology

# *EM2860*

# *USB Video Capture Device*

EM2860 Supports Video Decoder, Audio Decoder, and VBI



*Hardware Specification*

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# Features

## No external memory required

## Flexible Video Input Port

8-bit video input port
Support up to 1.3 M pixel CMOS sensor in Bayer RGB format
Interlace and non-interlace video
CCIR-601 4:2:2 YUV with external sync and field ID
CCIR-656 YUV with embedded sync and field ID

## Programmable Video Timing Generator

Generate clock, H-sync and V-sync for CMOS sensor

## Bayer RGB Color Processor

Black clamping
Gamma correction
Bayer pattern filtering
Gain and offset adjustment in RGB space
9-window image statistics collection for auto exposure and auto white balance
Defect pixel compensation

## YUV Color Processor

Gain and offset adjustment in YUV space
Sharpness enhancement

## Video Scaler

Random-ratio down scaling in X and Y directions
High fidelity color reproduction by the scaler

## VBI Capture

Raw VBI capture
Sliced VBI capture

## Audio Interface

Support AC97 CODEC
Support $I^2S$ device
Software direct access to AC97 CODEC registers
Support audio sample rates of 48K, 44.1K, 32K, 16K, and 8K.
Support USB Audio Class control and streaming

## Remote Controller Infrared Sensor Interface

Support NEC and RC5 remote control protocols

## USB Port

Integrated USB 2.0 PHY with High-Speed and Full-Speed Transceivers
Second generation USB 2.0 PHY with reduced power
USB 2.0 and 1.1 compliant

Support Iso-chronous audio pipe up to 0.2 MB/sec
Support Iso-chronous video pipe up to 30 MB/sec
Support Iso-chronous transport stream pipe up to 3 MB/sec

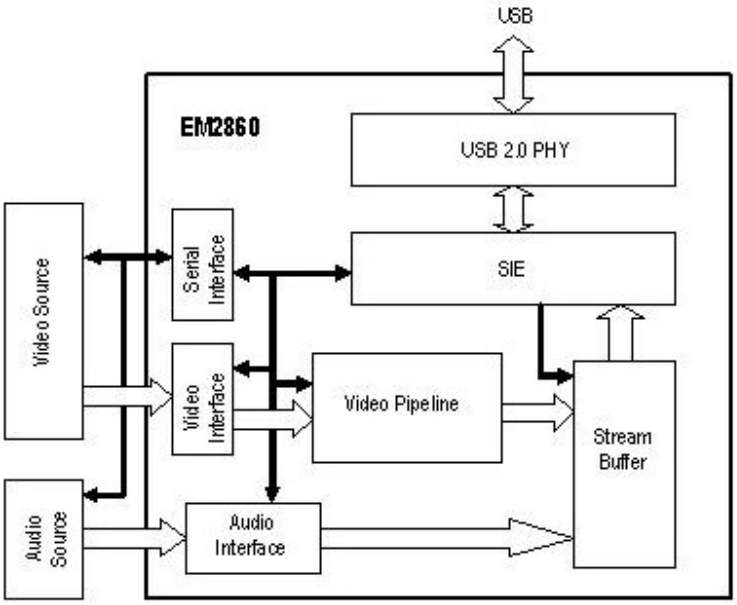
## EEPROM Interface

Support 256, 512, 1024 or 2048-byte 2-wire serial EEPROM
Use EEPROM to store chip configurations and USB descriptors
Customized Vendor ID and Product ID
Customized Vendor String, Product String, and Serial Number String
Software may use EEPROM to store board configurations
Software may use EEPROM to store defect pixel coordinates

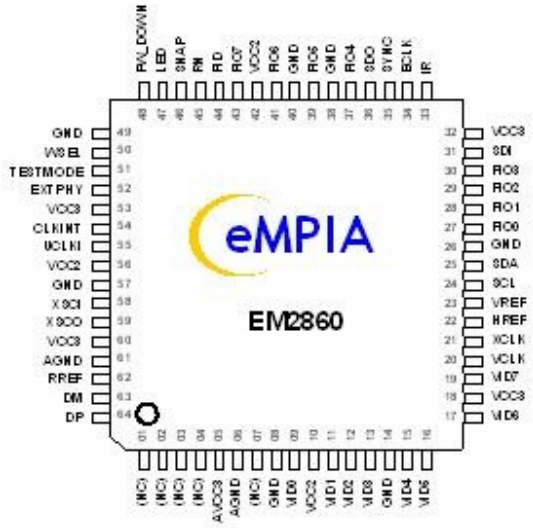
## Miscellaneous

2-wire serial bus to program front-end video/audio devices
Power-down control to front-end video/audio devices
8 general-purposed I/O ports
Snap shot button input
LED control output
0.22 micron, 2.5V Core, 3.3V I/O CMOS process
64-pin LQFP package

## Functional Block Diagram




## Pin Assignments



# General Description

EM2860 USB Video Capture Device (UVCD) is a highly integrated VLSI that provides a cost-effective solution for video capture applications on USB 2.0. Typical applications of this device are:

- *CMOS PC-Camera*
- *NTSC/PAL Video Capture*

As illustrated in the functional block diagram, an USB video subsystem consists of the UVCD, a video source, and optionally an audio source. The video source can be a CMOS sensor or an NTSC/PAL video decoder. The audio source can be an AC97 codec or an $I^2S$ stereo decoder. The USB host configures (programs) the video/audio source via the 2-wire serial bus or the AC97-link. Source video stream is transferred to the UVCD via the 8-bit video bus. Source audio stream is transferred to the UVCD via the AC97-link or the $I^2S$ bus.

As shown in the functional block diagram, the UVCD consists of 7 main blocks.

- *Video Interface*
- *Video Pipeline*
- *Audio Interface*
- *Stream Buffer*
- *Serial Interface Engine*
- *USB 2.0 PHY*
- *2-Wire Serial Interface*

## Video Interface

The Video Interface Block receives video data from external video source. Video clock (VCLK) and reference signals (VREF, HREF) from the video source are used to strobe incoming video data. CCIR-656 with embedded FID, VREF and HREF is also supported.

From the incoming video, a rectangular video sub-block is selected for feeding the next block, Video Pipeline.

The Video Interface Block also includes a video timing generator that generates HREF and VREF for slave-mode CMOS sensor.

## Video Pipeline

The Video Pipeline Block performs the following operations.

- *Black Clamping*
- *Gamma Correction*
- *RGB Gain and Offset*
- *Defect Pixel Compensation*
- *Up-Sampling 8-bit Bayer to 24-bit RGB,*
- *Color Space Conversion to YUV,*
- *Pixel Accumulation for AE and AWB*
- *Down Scaling*
- *Sharpness Enhancement*
- *Contrast, Brightness, and Saturation Adjustments*
- *UV Offset Adjustments*
- *Output Formatting*

- *Image Compression*

After the above operations, the compressed video is stored into the Stream Buffer.

## Audio Interface

The Audio Interface Block contains an AC97 controller and an $I^2S$ slave. Only one is enabled by configuration settings in EEPROM.

The AC97 controller interfaces with an external AC97 codec via 4-wire AC97-link. Supported audio sample rates are 48K, 44.1K, 32K, 16K, and 8K.

The $I^2S$ slave interfaces with an external $I^2S$ master via 3-wire $I^2S$ bus. The master is typically a stereo decoder. Supported audio sample rates are 48K, 44.1K, and 32K.

The Audio Interface Block converts the serial audio input to PCM16 format and stores into the Stream Buffer.

## Stream Buffer

The Stream Buffer stores the final audio and video data and delivers the data to the SIE upon request. The Stream Buffer is designed to sustain 24 MB/sec iso-chronous video transfer and 0.2 MB/sec iso-chronous audio transfer.

## Serial Interface Engine

The Serial Interface Engine can be divided into 2 sub-blocks: the SIE Controller on the front end and the Endpoint Logic on the back end. The SIE Controller manages USB packets and transactions. The Endpoint Logic implements endpoint specific logic required for video capture application. The SIE communicates with the USB 2.0 PHY via UTMI bus.

The UVCD complies with USB power management standard. When the USB bus stays idle for 3 mini seconds, the chip enters suspend mode and shuts down all internal clocks. The chip also sends out a power-down signal to external devices.

## USB 2.0 PHY

The USB 2.0 PHY includes 12-MHz Full-Speed transceivers, 480-MHz High-Speed transceivers, a PLL, and an UTMI controller. The transceivers are compliant to the USB 2.0 electrical specification. The PLL supplies clocks to the entire chip. The UTMI controller communicates with the SIE. The PHY has been optimized for low power. Furthermore, the PHY can be suspended by the SIE to conserve power.

## Serial Port and General I/O Port

The UVCD uses a two-wire serial bus to communicate with CMOS sensor or NTSC decoder. The serial port consists of SCL (clock) and SDA (data). Both are open-collector bi-directional ports. External pull-up resistors are required on both lines.

There are 8 general I/O ports. All general I/O ports are open-collector bi-directional pins. If a port is intended for output, it must be tied to external pull-up resistors.

# Pin Descriptions

## Video Interface

| Symbol | Pin No. | Type | Description |
|---|---|---|---|
| XCLK | 21 | O | Video synchronous clock output |
| VCLK | 20 | I | Video reference clock from video source |
| VREF | 23 | B | Vertical reference (sync) signal from video source in input mode.<br>Video timing generator vertical reference output in output mode. |
| HREF | 22 | B | Horizontal reference (sync) signal from video source in input mode.<br>Video timing generator horizontal reference output in output mode. |
| FID | 44 | I | Field ID from video source |
| VID7 | 19 | I | Video input data, bit 7 |
| VID6 | 17 | I | Video input data, bit 6 |
| VID5 | 16 | I | Video input data, bit 5 |
| VID4 | 15 | I | Video input data, bit 4 |
| VID3 | 13 | I | Video input data, bit 3 |
| VID2 | 12 | I | Video input data, bit 2 |
| VID1 | 11 | I | Video input data, bit 1 |
| VID0 | 9 | I | Video input data, bit 0 |

## Audio Interface

| Symbol | Pin No. | Type | Description |
|---|---|---|---|
| BCLK | 34 | I | AC97/$I^2S$ bit clock |
| SDI | 31 | I | AC97/$I^2S$ serial data input |
| SYNC | 35 | O | AC97 48 KHz fixed rate sample sync |
| SDO | 36 | O | AC97 serial data output |
| WSEL | 50 | I | $I^2S$ word select at audio sample rate |

## USB Interface

| Symbol | Pin No. | Type | Description |
|---|---|---|---|
| DP | 64 | B | USB differential data positive |
| DM | 63 | B | USB differential data negative |
| RREF | 62 | Analo | Connect reference resistor (12.1 KOhm, 0.1%) to Analog Ground |
| XSCI | 58 | Analo | Crystal oscillator input 12 MHz |
| XSCO | 59 | Analo | Crystal oscillator output 12 MHz |

## Serial Bus and Programmable I/O

| Symbol | Pin No. | Type | Description |
|---|---|---|---|
| SCL | 24 | B | Serial bus clock, require external pull-up resistor. |
| SDA | 25 | B | Serial data, require external pull-up resistor. |
| PIO7 | 43 | B | General I/O port 7, require external pull-up resistor in output mode. |
| PIO6 | 41 | B | General I/O port 6, require external pull-up resistor in output mode. |
| PIO5 | 39 | B | General I/O port 5, require external pull-up resistor in output mode. |
| PIO4 | 37 | B | General I/O port 4, require external pull-up resistor in output mode. |
| PIO3 | 30 | B | General I/O port 3, require external pull-up resistor in output mode. |
| PIO2 | 29 | B | General I/O port 2, require external pull-up resistor in output mode. |
| PIO1 | 28 | B | General I/O port 1, require external pull-up resistor in output mode. |
| PIO0 | 27 | B | General I/O port 0, require external pull-up resistor in output mode. |

## Remote Control Infrared Sensor Interface

| Symbol | Pin No. | Type | Description |
|---|---|---|---|
| IR | 33 | I | Infrared sensor signal |

## Miscellaneous

| Symbol | Pin No. | Type | Description |
|---|---|---|---|
| RN | 45 | I | Chip reset input. Active low. Connect to power-up RC circuit. |
| SNAP | 46 | I | Connect to snapshot button |
| LED | 47 | O | Connect to LED |
| PW_DOW | 48 | O | Power down external devices. |
| TESTMO | 51 | I | Put the chip in test mode. Normally tie to GND |
| EXTPHY | 52 | I | Select and use external PHY. Normally tie to GND |
| CLKINT | 54 | I | Select and use internal PLL. Normally tie to 3.3V VCC |
| UCLKI | 55 | I | Chip clock input when CLKINT=0. Normally tie to GND |

## Power and Ground

| Symbol | Pin No. | Type | Description |
|---|---|---|---|
| AVCC3 | 5, 60 | Power | 3.3V Analog Power |
| AGND | 6, 61 | Groun | Analog Ground |
| VCC3 | 18, 32, 53 | Power | 3.3V Digital Power |
| VCC2 | 10, 42, 56 | Power | 2.5V Digital Power |
| GND | 8, 14, 26, 38, 40, 49, 57 | Groun d | Digital Ground |
| (NC) | 1, 2, 3, 4, 7 | | No connect to internal die |

## EEPROM Data Structure

EEPROM contains hardware configuration information. After reset by RN, the UVCD reads the EEPROM and uses the information to configure the chip. The first four bytes of the EEPROM are Key to the EEPROM. If the EEPROM is absent or the Key is invalid, the UVCD is configured with a set of default values.

| Addr. | Data Definition | Default |
|---|---|---|
| 00H | Key Byte 0 = 1AH | - |
| 01H | Key Byte 1 = EBH | - |
| 02H | Key Byte 2 = 67H | - |
| 03H | Key Byte 3 = 95H | - |
| 04H | USB Vendor ID Low Byte | 1AH |
| 05H | USB Vendor ID High Byte | EBH |
| 06H | USB Product ID Low Byte | * |
| 07H | USB Product ID High Byte | * |
| 08H | Chip Configuration Low Byte<br>D[7] Class audio or vendor audio<br>0 – Inform the host that the chip is USB audio class device<br>1 – Inform the host that the chip is vendor specific audio device<br>D[6] USB audio class volume control capability when audio source is $I^2S$ device. When audio source is AC97, the chip is always capable of volume control regardless of the state of this bit.<br>0 – Inform the host that the chip is not capable of volume control.<br>1 – Inform the host that the chip is capable of volume control.<br>D[5:4] Audio Configuration<br>00 – No audio on board.<br>01 – AC97 audio on board with 5 sample rates: 48K, 44.1K, 32K, 16K, and 8K.<br>10 – $I^2S$ audio on board with 3 sample rate: 32K, 16K, and 8K.<br>11 – $I^2S$ audio on board with 5 sample rates: 48K, 44.1K, and 32K, 16K, and 8K.<br>D[3] USB Remote Wakeup Capable when set to 1<br>D[2] USB Self Power Capable when set to 1. If the chip is configured to be Self Power Capable, PIO7 becomes self power status input.<br>D[1:0] USB Max Power Select<br>00 – USB Max Power 500 mA<br>01 – USB Max Power 400 mA<br>10 – USB Max Power 300 mA<br>11 – USB Max Power 200 mA | ** |
| 09H | Chip Configuration High Byte<br>D[7:5] Reserved. Set to 0.<br>D[4] Transport stream on board<br>0 – Inform the host that the chip supports transport stream.<br>1 – Inform the host that the chip does not support transport stream.<br>D[3:2] Transport stream iso-chronous request interval<br>00 – Inform the host that request interval is 0 (one request every micro-frame)<br>01 – Inform the host that request interval is 1 (one request every 2 micro-frames)<br>10 – Inform the host that request interval is 2 (one request every 4 micro-frames)<br>11 – Inform the host that request interval is 3 (one request every 8 micro-frames)<br>D[1:0] Transport stream MaxPacketSize select<br>00 – Inform the host that MaxPacketSize is 188*1 bytes<br>01 – Inform the host that MaxPacketSize is 188*2 bytes<br>10 – Inform the host that MaxPacketSize is 188*3 bytes<br>11 – Inform the host that MaxPacketSize is 188*4 bytes | 00H |

| | | |
|---|---|---|
| 0AH | Board Configuration Low Byte<br>To be defined by Software Architect | 00H |
| 0BH | Board Configuration High Byte<br>To be defined by Software Architect | 00H |
| 0CH | String 1 Descriptor Pointer<br>Starting address of String 1 Descriptor in the EEPROM | 00H |
| 0DH | String 1 Descriptor Length<br>Number of bytes of String 1 Descriptor in the EEPROM | 00H |
| 0EH | String 2 Descriptor Pointer<br>Starting address of String 2 Descriptor in the EEPROM | 00H |
| 0FH | String 2 Descriptor Length<br>Number of bytes of String 2 Descriptor in the EEPROM | 00H |
| 10H | String 3 Descriptor Pointer<br>Starting address of String 3 Descriptor in the EEPROM | 00H |
| 11H | String 3 Descriptor Length<br>Number of bytes of String 3 Descriptor in the EEPROM | 00H |
| 12H | String Index Table<br>D[7:6] Reserved. Set to 0.<br>D[5:4] Serial Number String Descriptor Index<br>D[3:2] Product String Descriptor Index<br>D[1:0] Vendor String Descriptor Index | 00H |
| 24H | Minimum Audio Volume (2's complement number)<br>This is audio class minimum audio volume to report to the host so that the host will not set any volume smaller than this. | F0H |
| 25H | Maximum Audio Volume (2's complement number)<br>This is audio class maximum audio volume to report to the host so that the host will not set any volume bigger than this. | 10H |

## Note:

* Default Product ID is listed below:

| Chip Type | Product ID (w.o. audio) | Product ID (w. audio) |
|---|---|---|
| EM2860 | 2860H | 2861H |

** Default Chip Configuration Low Byte = 00H if PIO7 is pulled down with a resistor.
Default Chip Configuration Low Byte = 10H if PIO7 is pulled up with a resistor.

# Electrical Specifications

## Absolute Maximum Ratings

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Power Supply Voltage | -0.3 | $V_{CC}$+0.3 | V |
| Voltage on any input | -0.3 | 5.5 | V |
| Operating Temperature (Ambient) | 0 | 70 | $^{o}$C |
| Storage Temperature | -40 | 150 | $^{o}$C |

Note:
1. Stress beyond those listed may cause permanent damage to the device.
2. Input pins are 5V tolerant.

## DC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC2}$ | Core Supply Voltage | | 2.25 | 2.5 | 2.75 | V |
| $V_{CC3}$ | I/O Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | Input High Voltage | $V_{cc3}$ = 3.3V | 2.0 | | | V |
| $V_{IL}$ | Input Low Voltage | $V_{cc3}$ = 3.3V | | | 0.8 | V |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V |
| $I_{CC}$ | Operating Supply Current | | | | 120 | mA |
| $I_{CCS}$ | Suspend Supply Current | | | | 250 | μA |
| $C_{IN}$ | Input Capacitance | | | 3.5 | | pF |
| $C_{OUT}$ | Output Capacitance | | | 3.5 | | pF |

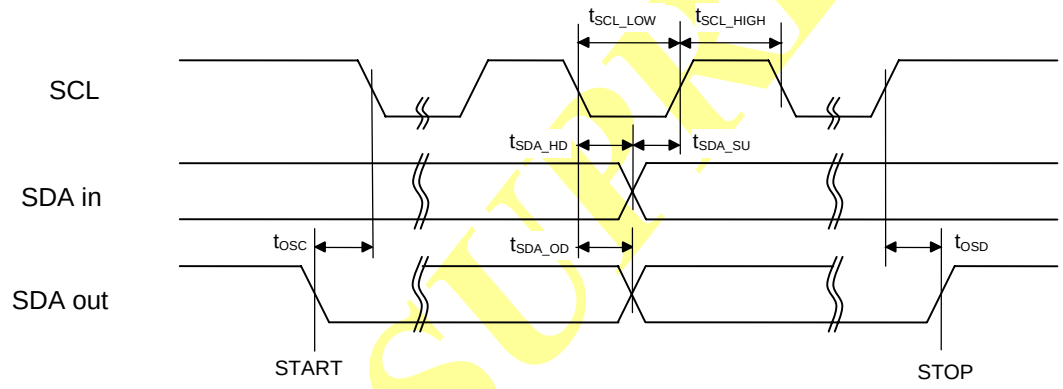
## AC Characteristics

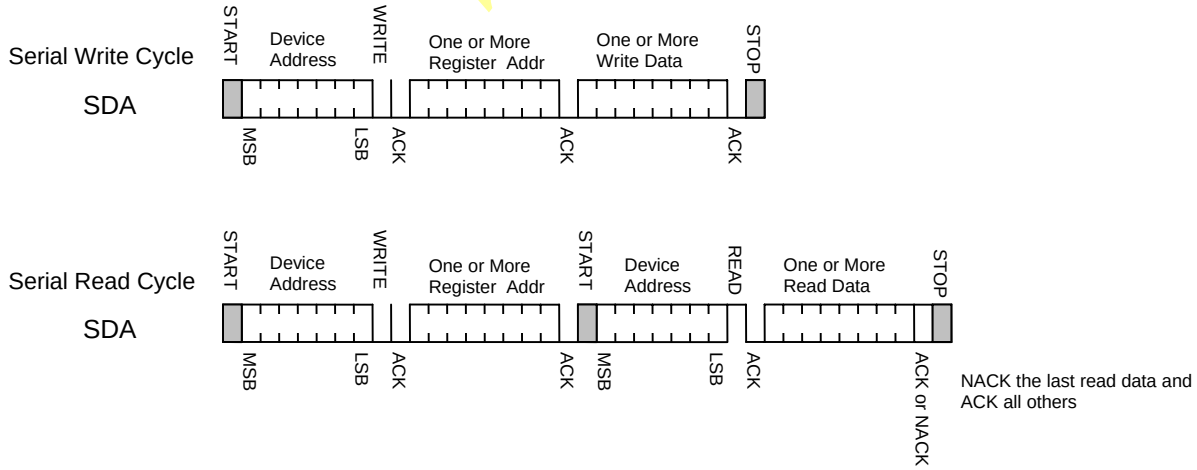
| Symbo | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{XTAL}$ | Crystal Frequency at XSCI, XSCO | | 12 | | MHz |

## Serial Bus Timing

Conditions: 100 KHz SCL; 4.7 KOhm pull up; 100 pF load;

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL Frequency | | 100 | | KHz |
| $t_{SCL\_LOW}$ | SCL Low Pulse Width | 4.7 | | | µs |
| $t_{SCL\_HIGH}$ | SCL High Pulse Width | 4.0 | | | µs |
| $t_{OSC}$ | SDA to SCL Output Delay at START and STOP | 4.0 | | 7.0 | µs |
| $t_{OSD}$ | SCL to SDA Output Delay at START and STOP | 4.0 | | 7.0 | µs |
| $t_{SDA\_OD}$ | SDA Output Delay | 4.0 | | 7.0 | µs |
| $t_{SDA\_SU}$ | SDA Input Setup Time | 0 | | | ns |
| $t_{SDA\_HD}$ | SDA Input Hold Time | 100 | | | ns |

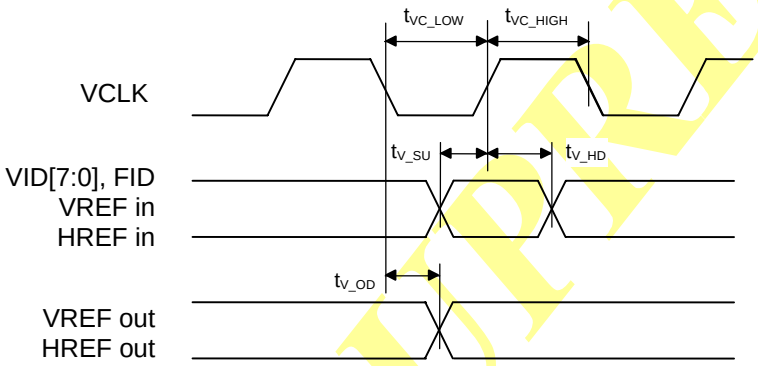


## Video Interface Timing

Conditions: 50 pF load

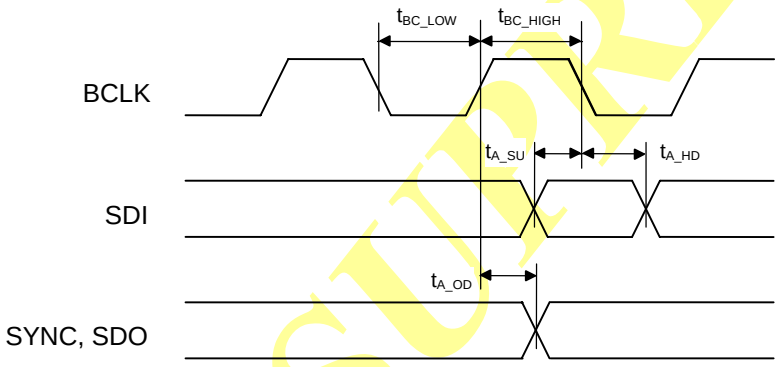
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{VCLK}$ | VCLK Frequency | | | 29 | MHz |
| $t_{VC\_LOW}$ | VCLK Low Pulse Width | 15 | | | ns |
| $t_{VC\_HIGH}$ | VCLK High Pulse Width | 15 | | | ns |
| $t_{V\_OD}$ | Video Output Delay | 0 | | 10 | ns |
| $t_{V\_SU}$ | Video Input Setup Time | 10 | | | ns |
| $t_{V\_HD}$ | Video Input Hold Time | 10 | | | ns |



## AC97-Link Timing

Conditions: 50 pF load

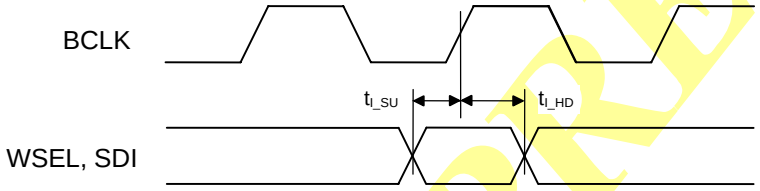
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{BCLK}$ | BCLK Frequency | | 12.288 | | MHz |
| $f_{SYNC}$ | SYNC Frequency | | 48 | | KHz |
| $t_{BC\_LOW}$ | BCLK Low Pulse Width | 36 | | 45 | ns |
| $t_{BC\_HIGH}$ | BCLK High Pulse Width | 36 | | 45 | ns |
| $t_{A\_OD}$ | AC97 Data Output Delay | 0 | | 15 | ns |
| $t_{A\_SU}$ | AC97 Data Input Setup Time | 10 | | | ns |
| $t_{A\_HD}$ | AC97 Data Input Hold Time | 10 | | | ns |

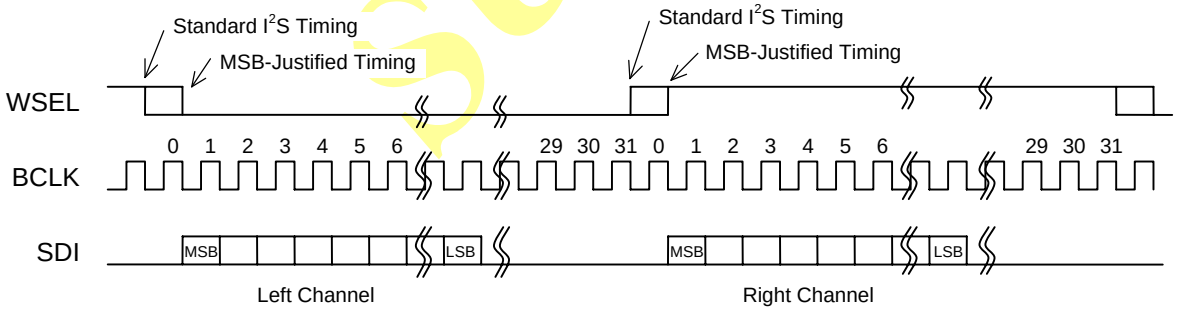


## I²S Timing

Conditions: 50 pF load

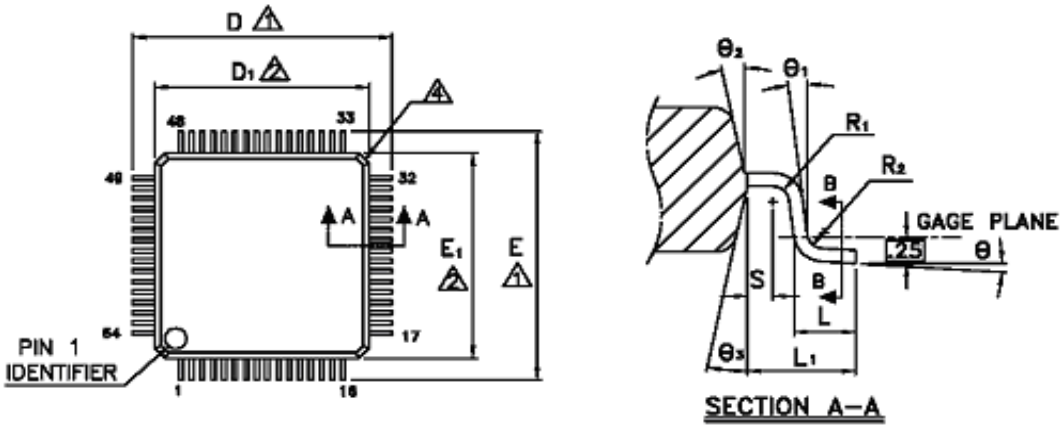
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{BCLK}$ | BCLK Frequency | | | 3072 | KHz |
| $f_{WSEL}$ | WSEL Frequency | | | 48 | KHz |
| | BCLK Duty Cycle | | 50 | | % |
| $t_{I\_SU}$ | I²S Data Input Setup Time | 10 | | | ns |
| $t_{I\_HD}$ | I²S Data Input Hold Time | 10 | | | ns |

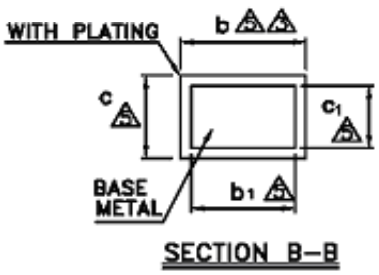


# Packaging Information

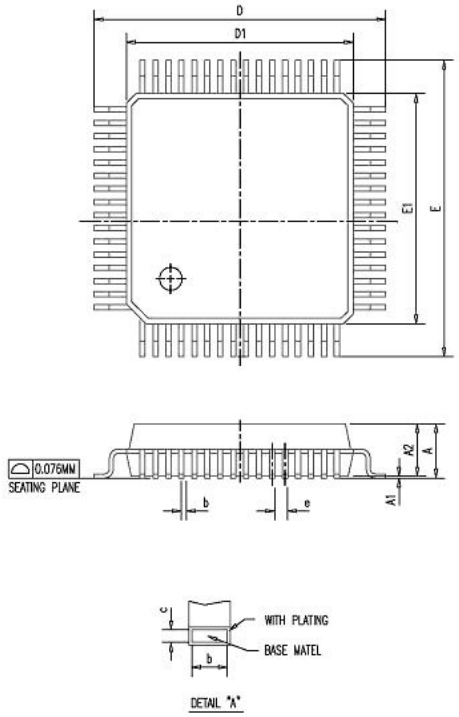
## 64-pin (10x10) QFP Mechanical Drawing

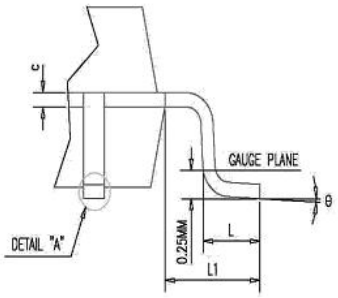



| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.60 | — | — | 0.063 |
| $A_1$ | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.012 | 0.015 | 0.018 |
| $b_1$ | 0.17 | 0.20 | 0.23 | 0.012 | 0.014 | 0.016 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| $c_1$ | 0.09 | — | 0.16 | 0.004 | — | 0.006 |
| D | 12.00 BSC | | | 0.472 BSC | | |
| $D_1$ | 10.00 BSC | | | 0.394 BSC | | |
| E | 12.00 BSC | | | 0.472 BSC | | |
| $E_1$ | 10.00 BSC | | | 0.394 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | 1.00 REF | | | 0.039 REF | | |
| $R_1$ | 0.08 | — | — | 0.003 | — | — |
| $R_2$ | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| S | 0.20 | — | — | 0.008 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $\theta_1$ | 0° | — | — | 0° | — | — |
| $\theta_2$ | 12°TYP | | | 12°TYP | | |
| $\theta_3$ | 12°TYP | | | 12°TYP | | |

## 64-pin LQFP (7X7) Mechanical Drawing




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 8.90 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| D1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.280 |
| E | 8.90 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| E1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.280 |
| e | 0.40 BSC. | | | 0.016 BSC. | | |
| b | 0.16 BSC. | | | 0.006 BSC. | | |
| c | 0.127 TYP. | | | 0.005 TYP. | | |
| L | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| L1 | 1.00 REF. | | | 0.039 REF. | | |
| θ | 0 | 3.5 | 7 | 0 | 3.5 | 7 |
| JEDEC | | | | | | |